Charge Recovery Implementation of an Analog Comparator: Initial Results

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***Abstract*—This work introduces a charge recovery comparator circuit for low-power, low-frequency applications. For the first time, the principles of charge recovery logic, or adiabatic logic, are applied to an analog circuit. The comparator is designed and simulated in a $180\,\mathrm{nm}$ technology and compared to state of the art solutions. Post-extraction simulations show that the proposed comparator consumes only $46\,\mathrm{fJ}$ per conversion in the nominal PVT corner, while having a total area of $45\,\mu\mathrm{m}^2$. The proposed comparator consumes up to $70\,\%$ less power than a state of the art dynamic latch comparator.**

I. Introduction

In static CMOS, energy is dissipated by the pull-up and pull-down networks during the low-to-high and high-to-low transitions of the output, respectively. Charge is moved from the power source, V_{DD}, to the load capacitance, then discharged to ground. Charge recovery logic (CRL), also known as adiabatic logic, is a logic style aiming at recycling or recovering the energy that is usually discharged to ground during static CMOS operation [1]. One of the main features of charge recovery logic is the use of a power-clock. The power-clock is a periodic signal, usually a sine-wave, that provides both power and timing to the CRL gates. Depending on the particular logic family, the power-clock can be one, two, or more sine-waves, hence producing the common terminology of single-phase, two-phases, and four-phases power-clock. The power-clock enables charge to flow back and forth from the CRL gates, not dissimilarly from an LC oscillator, hence recycling part of the energy and providing power savings [2].

Figure 1 shows the current research status regarding circuits that use charge recovery principles. The term *DC supply* in Figure 1 is used for traditional circuits, analog or digital, that need a stable DC voltage to operate. In contrast, the term *Charge Recovery* is used to indicate circuits that use a power-clock and that recycles part of the energy that flows in the circuit. Charge recovery logic has been under active research for many years [1], and fairly complex digital circuits such as FIR filters are silicon proven [3]. To the authors' knowledge, however, no research has been conducted on charge recovery for analog circuits. This work addresses this gap, introducing an analog comparator that shows charge recovery behavior and achieves power savings. The proposed circuit is designed and simulated in a CMOS $180\,\mathrm{nm}$ technology.

The target application in biomedical devices selected for performance assessment of the charge-recycling comparator is

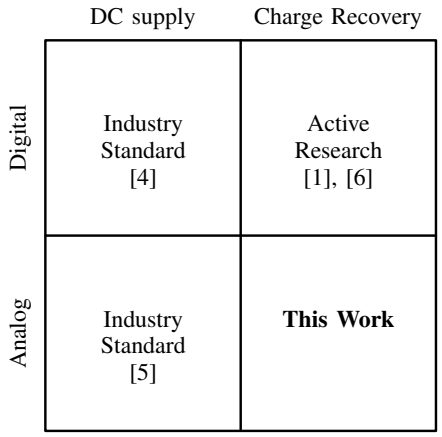

Fig. 1. Status of research on charge recovery circuits

an area that has accentuated value within the past decade. In particular, the comparators employed in the ADCs reported in [7], [8] are used as a baseline for comparison with the proposed charge-recycling comparator. The comparator in these biomedical devices operate at the kHz range, and are useful for converting physiological signals such as EEG, ECG, et cetera. The ADC in [7] uses a $0.6\,\mathrm{V}$ supply voltage in a $180\,\mathrm{nm}$ technology, well under the nominal supply. The ADC in [8], on the other hand, uses a nominal voltage supply. The comparator in [8] consumes an order of magnitude more energy than the comparator in [7], as estimated from the reported power consumption. The proposed comparator, when operated at the nominal $1.8\,\mathrm{V}$, consumes $70\,\%$ less energy than the comparator in [8]. On the other hand, when operated at $0.6\,\mathrm{V}$, the proposed comparator consumes $60\,\%$ less power than the near-threshold comparator in [7].

Section II shows a traditional charge recovery logic buffer. Section III introduces the proposed charge recovery comparator and its main building blocks. Section IV shows the layout of the proposed comparator and post-extraction results.

II. A charge recovery buffer gate

As an introduction to charge recovery operation, a simple buffer gate is considered in this section. For the sake of

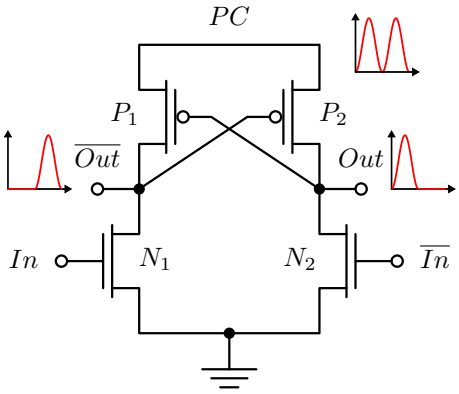

Fig. 2. The ECRL buffer

simplicity, the Efficient Charge Recovery Logic family, or ECRL, is used [9], but the same principles apply to other CRL families as well. Figure 2 shows the circuit of an ECRL buffer, which operates analogously to a sense amplifier. The waveforms in Figure 2 show two power-clock periods of an ideal ECRL buffer. At the beginning of a cycle, the power-clock PC and the output nodes Out and $\overline{Out}$ are low, while the input In is high and $\overline{In}$ is low. As the power-clock PC increases, in what is called the evaluation phase, the two cross-coupled PMOS transistors P_1 and P_2 start to conduct some current. Transistor N_1, driven by the high input In, makes sure that $\overline{Out}$ is kept at ground, while Out follows the power-clock PC thanks to P_2. Once the cross-coupled PMOS transistors start to amplify the difference between Out and $\overline{Out}$, the input In is no longer needed and can return low. When the power-clock PC starts to decrease, in what is called the recovery phase of the power-clock, P_2 discharges Out to the power-clock, recovering the charge that was present on the load capacitance on node Out. During the next cycle the inputs are inverted, In is low and $\overline{In}$ is high, and the outputs are the opposite, as well.

III. The Proposed Comparator

The proposed comparator is composed of two major building blocks: the decision circuit and the output buffer. The former discriminates whether the input is larger or smaller than the reference voltage, while the latter converts this information to a full-swing voltage signal. Both the decision circuit and the output buffer use charge-recovery principles and achieve very low power consumption.

A. The decision circuit

Figure 3 shows the schematic of the decision circuit, based on the ECRL gate introduced in Section II. The key difference with respect to the ECRL gate of Figure 2 is that the sources of N_1 and N_2 are tied to a capacitor C_S rather than ground. This difference is the key to accommodate a wide range for the reference voltage V_{REF}. The voltage V_S is brought by N_2 to $V_{REF} - V_{TN}$, where V_{TN} is the threshold voltage of the NMOS transistors. Since the sources of N_1 and N_2 are

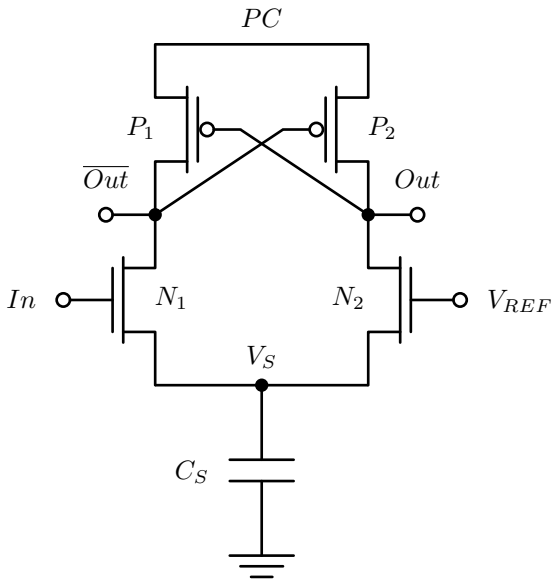

Fig. 3. The decision circuit of the proposed comparator

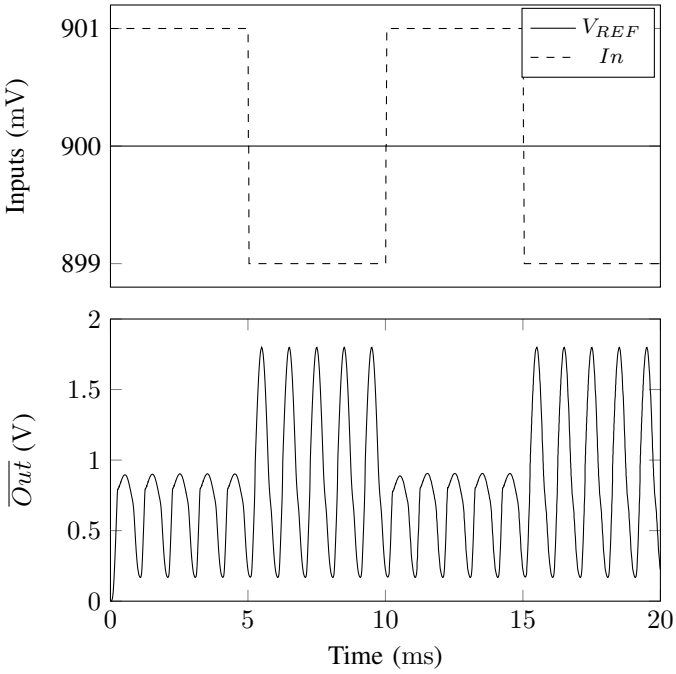

Fig. 4. The output of the decision circuit at 1 kHz and with $V_{REF} = 0.9\,\mathrm{V}$

one threshold voltage lower than V_{REF}, both transistors are in weak to strong inversion. The minimum V_{REF} for correct operation is then around the NMOS threshold voltage V_{TN}. When this requirement is met, N_1 and N_2 behave similarly to the classic differential pair [5] of an operational amplifier. In a conventional differential pair, replacing the traditional current source with the capacitor C_S would lead the circuit to saturate. The small leakage currents of the NMOS transistors would be enough to charge the capacitor C_S to larger and

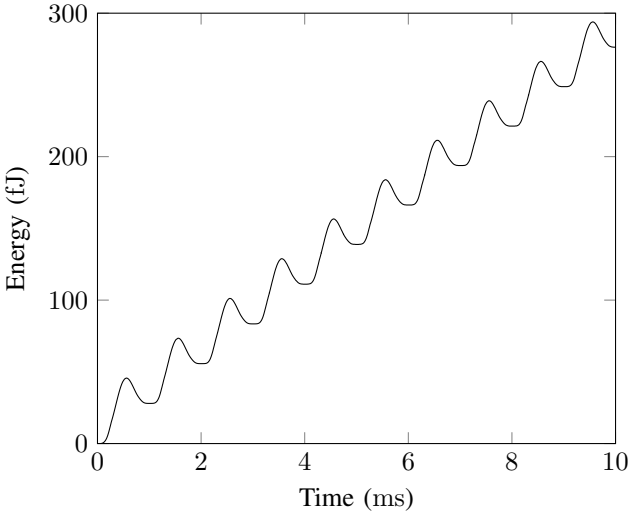

Fig. 5. The energy profile of the post-extraction simulated CRL comparator

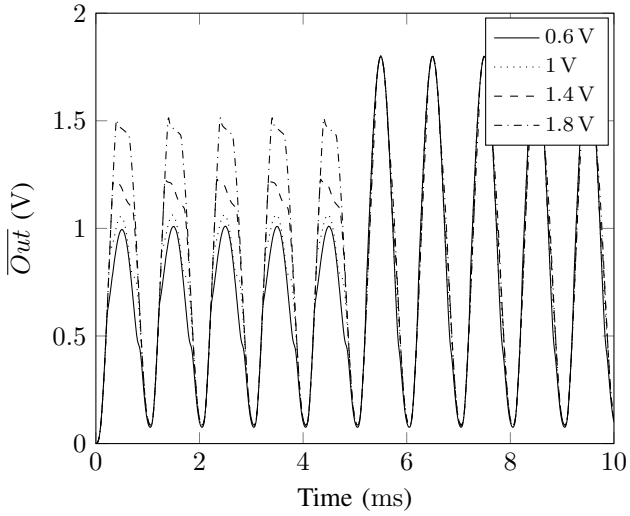

Fig. 6. The output of the decision circuit for different V_{REF}

larger voltages. In the circuit of Figure 3, this phenomenon does not happen, and the circuit does not saturate thanks to the operation of the power-clock PC. When PC is low, transistor N_2 discharges C_S through P_2, down to the PMOS threshold voltage V_{TP}. As in the gate of Figure 2, the two cross-coupled PMOS transistors amplify the the action of the NMOS transistors and provide the differential output.

Figure 4 shows the inputs and output of the decision circuit, at a frequency of $1\,\mathrm{kHz}$ and a reference voltage of $V_{DD}/2 = 0.9\,\mathrm{V}$. The decision circuit is able to discriminate the input signal when the latter is high or lower than the reference voltage by only $1\,\mathrm{mV}$. The minimum reference voltage for the decision circuit to be functional is, as expected, around the NMOS threshold voltage V_{TN}, roughly $0.6\,\mathrm{V}$. Figure 5 shows the energy profile of the comparator of Figure 3, after a custom layout and parasitics extraction in $180\,\mathrm{nm}$ technology. The energy is effectively recycled back to the power source, decreasing the overall consumption.

B. The output buffer

Because of the capacitor C_S of Figure 3, the output of the decision circuit depends on the voltage reference V_{REF}. In particular, the *low* voltage level at the output varies substantially. Figure 6 shows the output of the decision circuit for a reference voltage from $V_{REF} = V_{TN} \approx 0.6\,\mathrm{V}$ to $V_{REF} = V_{DD} = 1.8\,\mathrm{V}$. The low value for the output goes from $1\,\mathrm{V}$ when $V_{REF} = 0.6\,\mathrm{V}$ to $1.5\,\mathrm{V}$ when $V_{REF} = 1.8\,\mathrm{V}$. Such a voltage cannot be directly used to drive a charge recovery logic gate such as the one in Figure 2, because it would drive both the NMOS N_1 and N_2 to linear region. In order to convert the output signal of Figure 6 to a usable level, the output buffer of Figure 7 is proposed. This output buffer is based on the *Pass-transistor Adiabatic Logic* [10], or PAL, buffer, with the addition of two level-shifter NMOS transistors, N_3 and N_4. These two transistors lower the voltage level of the decision circuit, Figure 6, that can then be used

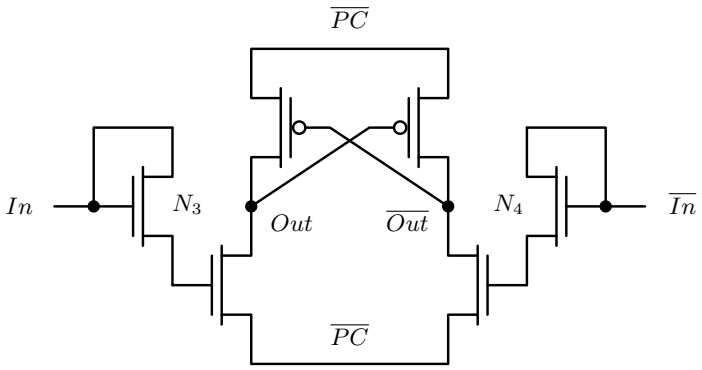

Fig. 7. The designed output buffer

to drive a regular PAL or ECRL buffer gate. Depending on the threshold voltage of the particular technology and the operating frequency, one or more level-shifter NMOS transistors can be stacked to achieve the desired voltage offset. The output buffer uses charge recovery principles as well, making the whole comparator a charge recovery circuit.

IV. LAYOUT AND EXTRACTION

Since the decision circuit of Figure 3 works at low-power and with the NMOS transistors close to the threshold voltage, it is paramount that the transistors be matched to each other. The layouts for both the decision circuit and the output buffer are custom designed in a $180\,\mathrm{nm}$ technology. The area for the decision circuit, as shown in Figure 8, is $25\,\mu\mathrm{m}^2$. The layout is kept as symmetrical as possible, in order to have symmetrical parasitics. The area for the layout of the output buffer of Figure 7 is $20\,\mu\mathrm{m}^2$, bringing the total area of to $45\,\mu\mathrm{m}^2$. As a reference, the reported area for the dynamic latch comparator in [7] is $178\,\mu\mathrm{m}^2$, four times ($4\times$) the area of the proposed comparator.

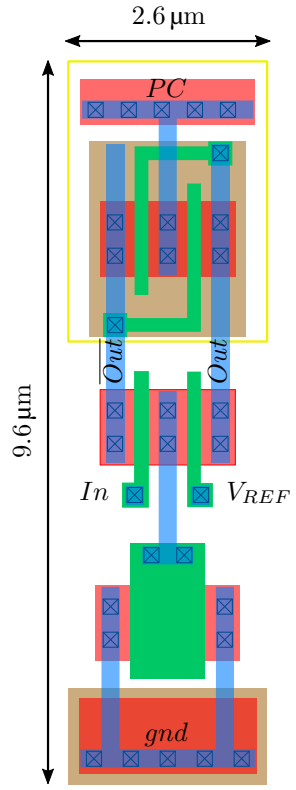

Fig. 8. The layout of the decision circuit of Figure 3

TABLE I
POST-EXTRACTION POWER CONSUMPTION AT 1 kHz

Corner	@ 1.8 V (pW)	@ 0.6 V (pW)
tt	45.3	6.97
ss	43.6	6.48
sf	46.9	6.78
fs	44.2	6.31
ff	48.4	6.53
Average	45.7	6.61

Table I reports the power consumption computed from the post-extraction simulations of the complete decision circuit and buffer. The post-extraction simulations are performed at two voltage nodes: 1) the power-clock has an amplitude equal to the nominal voltage of the technology, 1.8 V, and 2) the power-clock has an amplitude of 0.6 V, hence operating the circuit at near-threshold voltage for lower power dissipation. On average, the proposed comparator consumes 45.7 pW when operated at the nominal voltage and 6.61 pW when operated at the near-threshold voltage. At 1 kHz, the proposed comparator consumes 45.7 fJ and 6.61 fJ per conversion for the two voltage nodes of 1.8 V and 0.6 V, respectively. The proposed comparator consumes 85 % less energy when operated at near-threshold voltage with respect to the nominal voltage operation.

Table II shows a comparison of the proposed comparator with respect to two state of the art comparators that are

TABLE II
LITERATURE COMPARISON

	[8]	[7]	This Work	
Technology (nm)	180	180	180	180
Voltage (V)	1.5	0.6	1.8	0.6
Frequency (kHz)	110	20	1	1
Power (pW)	19000	338	46	6.61
Energy (fJ)	173	16.9	46	6.61

used in two silicon proven ADCs [8], [7]. The power consumptions of the state of the art comparators are computed from the referenced papers, since only the total power and the comparator percentage are reported. For a comparison at the nominal voltage, the proposed comparator consumes 46 fJ per conversion while the state of the art comparator in [8] consumes 173 fJ per conversion, a 70 % decrease. At the near-threshold voltage, the proposed comparator consumes 6.61 fJ per conversion while the state of the art comparator in [7] consumes 16.9 fJ per conversion, a 60 % decrease.

V. CONCLUSION

This paper presents an analog comparator that has lower power consumption and a smaller footprint with respect to state of the art solutions. The discussion given in this paper is the first to propose and illustrate a comparator design that achieves very low-power by applying charge recovery logic principles to analog circuits. Performance comparison with respect to recent biomedical circuit implementations of different comparators demonstrate energy savings between 60 % and 70 % (at a lower frequency of 1 kHz). Future research is necessary toward frequency scaling for high-performance applications, noise evaluation, and silicon validation.

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