Ying Teng

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Summary of Qualifications

- 4 years Ph.D. research experience on Digital Circuit Physical Design and Optimization, including: Floorplan, Placement, Clock tree/Mesh Synthesis and Optimization, Routing Methodologies, Extraction Modeling and Timing Analysis.
- 1 year industry experience and 4 years Ph.D. research experience on Analog and Mixed-signal Circuit Design: Simulation, Layout, Extraction and Verification (using Cadence/Synopsys/Mentor tools).
- Strong research experience on Custom Circuit Design Automation.
- Familiar with Data Structures, Algorithms and Graph Theory.

Education

Drexel University **June 2014 (expected)**

- Ph.D., Electrical and Computer Engineering (3.91/4).
  Dissertation: "Low power Clock Distribution Network Design",
  Advisor: Dr. Baris Taskin

Tianjin University, Tianjin, China **March 2007**

- M.S., Electronic and Information Engineering.
  Area of Study: Analog and mixed signal integrated circuit design

Tianjin University, Tianjin, China **June 2004**

- B.S., Electronic and Information Engineering (rank 2 out of 90)

Skills

- Cadence: Virtuoso, Encounter Design Implementation System, SKILL Language;
- Synopsys: HSPICE, Design Compiler, IC Compiler, PrimeTime, Hercules, StarRC;
- Mentor: HDL Designer, Modelsim, Calibre;
- C/C++, Perl, Tcl, MATLAB, Python;
- VerilogHDL, VHDL

Experience

Research Assistant, VLSI Laboratory, Drexel University, Philadelphia, PA. **September 2009 - Current**

- Mixed-signal circuit design of resonant rotary travelling wave oscillator.
  - Proposed the circuit topology "ROA-brick": Interconnect modeling (Virtuoso/ICC/HSPICE), extraction (StarRC/QRC), system design (Virtuoso/EDI/Perl), and custom VLSI static timing analysis (HSPICE/Perl).
  - Proposed the circuit topology "Sparse-ROA": Physical design (HSPICE/Perl), clock topology and distribution network design (more than 2000 lines of C++/DEF/HSPICE).
  - Proposed a dynamic frequency divider for resonant clocks: Mixed-signal circuit design (Drexel Invention disclosure).
- Physical digital design and optimization of resonant and PLL-based designs.
  - Proposed a Sparse-ROA-based clock distribution network optimization method.
    - More than 10,000 lines of C++/Perl code;
    - Interoperable with Skill Language and Tcl/StarRC
  - Developed a complete backend automation flow using Cadence EDI, including:
    - Custom Perl/Scheme designs the resonant clocks.
    - Floorplan, Placement, regional Clock tree Synthesis and Routing of resonant-based circuits.
  - Clock mesh automation for PLL-based clocks:
    - Placement, CTS and Routing of more than 5,000 lines of C++/Perl code;
    - Interoperable with Synopsys Tcl/StarRC/HSPICE
- Chip tapeout experience
  - IBM 90nm technology IBM9LPRF for research projects Resonant Clocking and Wireless Interconnects: a 2mm*2mm mixed-signal circuit chip.
  - On Semiconductor 0.5um technology ON_C5N for graduate class project: 1.5mm*1.5mm mixed-signal circuit chip.

Teaching Assistant, Drexel University, Philadelphia, PA. **September 2009 - Current**

- ECE-C471/472/473 Custom VLSI Design I/II/III
- ECE-C474/475 ASIC Design I/II
- ECE-E421/422/434 Advanced Electronic Circuits
- ECE-C355 Computer Organization and Architecture
- ECE-E352 Analog Electronics

Junior Design Engineer, Micron Semiconductor Technology Co., Ltd, Shanghai, China. **March 2007-March 2008**

- Full custom DRAM integrated circuit design with a 90nm technology
  - Design analysis and verification of DLL (Digital locked loop).
  - Design and verification of power management circuits, including: Voltage reference, regulator.
  - Designed a charge pump (The charge pump was verified on silicon and integrated into one series of the DRAM circuit topology).
  - Timing verification of the DRAM Testmode circuit blocks.

Intern, Conexant Broadband Communication Co., Ltd, Shanghai, China. **July 2006 - January 2007**

- Performed the turbo codec IP core verification in the physical layer for HomePlug AV standard.

Publications

Journals:

1. J. Lu, **Y. Teng** and B. Taskin, "A Reconfigurable Clock Polarity Assignment Flow for Clock Gated Designs", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI),* vol. 20, issue 6, pp. 1002-1011, June 2012.
2. **Y. Teng** and B. Taskin, "Look-up Table Based Low Power Rotary Travelling Wave Oscillator Design Considering the Skin Effect", *Journal of Low Power Electronics (JOLPE),* Vol. 6, No. 4, pp. 491-502, Dec. 2010 (**Cover Feature**).

Conferences:

1. **Y. Teng** and B. Taskin, "Resonant Frequency Divider Design Methodology for Dynamic Frequency Scaling", in Proceedings of the *IEEE International Conference on Computer Design (ICCD),* Oct. 2013.
2. **Y. Teng** and B. Taskin, "Rotary Traveling Wave Oscillator Frequency Division at Nanoscale Technologies", in Proceedings of *ACM Great Lakes Symposium on VLSI (GLSVLSI),* May 2013, pp. 349-350.
3. **Y. Teng** and B. Taskin, "Sparse-Rotary Oscillator Array (SROA) Design for Power and Skew Reduction", in Proceedings of the *Design, Automation and Test in Europe (DATE),* March 2013, pp. 1229-1234.
4. **Y. Teng** and B. Taskin, "Clock Mesh Synthesis Method using Earth Mover's Distance under Transformations", in Proceedings of the *IEEE International Conference on Computer Design (ICCD),* October 2012, pp. 121-126.
5. **Y. Teng** and B. Taskin, "Synchronization Scheme for Brick-based Rotary Oscillator Arrays", in Proceedings of *ACM Great Lakes Symposium on VLSI (GLSVLSI),* May 2012, pp. 117-122.
6. **Y. Teng** J. Lu and B. Taskin, "ROA-brick Topology for Rotary Resonant Clocks", in Proceedings of the *IEEE International Conference on Computer Design (ICCD),* Oct. 2011, pp. 273-278.
7. **Y. Teng** and B. Taskin, "Process Variation Sensitivity of the Rotary Traveling Wave Oscillator", in Proceedings of the *IEEE International Symposium on Quality Electronic Design (ISQED),* Mar. 2011, pp. 236-242.
8. V. Honkote, A. More, **Y. Teng,** J. Lu and B. Taskin, "Interconnect Modeling, Synchronization and Power Analysis for Custom Rotary Rings", in Proceedings of the *International Conference on VLSI Design (VLSID),* Jan. 2011.

Awards and Honors

- **Invention disclosure Drexel University**: "Dynamic frequency divider for resonant clocks", 2013.
- **Hill Fellowship**, Drexel University, 2011–2012: Granted to 5 outstanding graduate students in the College of Engineering, the only female to receive this award in 2011.
- **Nihat Bilgutay Fellowship,** Drexel University, 2010–2011**:** Granted to two Ph.D. students in the Electrical and Computer Engineering Department.
- **Cover feature article:** *Journal of Low Power Electronics (JOLPE),* Dec. 2010

Relevant Coursework

- CMOS VLSI Design, Custom VLSI Design I/II/III, ASIC Design I/II; Computer Architecture; VHDL; CAD for VLSI Design I & II; Deep Submicron Systems; Introduction to RFIC.
- Data Structure and Algorithms; Computational Geometry; Program Tools and Environments.