Michael Lui

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Education

Ph.D. Candidate, Computer Engineering — Expected 2020
Electrical and Computer Engineering, Drexel University — Philadelphia, PA

BS/MS in Computer Engineering — June 2012
Electrical and Computer Engineering, Drexel University — Philadelphia, PA

Research Experience

Research Assistant, VLSI and Architecture Lab (VANDAL), September 2014-Present
Department of Computer and Electrical Engineering, Drexel University

- Research focus on workload guided hardware/software co-design methodologies
- Workload profiling and characterization methodologies leveraging dynamic binary instrumentation, static binary instrumentation, and hardware profiling
- Design space exploration for many-core and accelerator-centric architectures
- HLS methodologies for domain specific applications
- Administrates research computing cluster

Intern, AI Infra Foundation, Research, September 2019-November 2019
Extern Researcher, AI Infra Foundation, Research, January 2019-Present
Facebook, Cambridge, MA

- Characterize and profile distributed AI inference of recommendation ML models
- Study and analyze compute and latency overheads in distributed implementation
- Instrument production Caffe2 predictor servers to generate distributed traces for post-processing and visual analysis
- Study optimizations Caffe2- and system-level optimizations, e.g. model size and storage, network-infrastructure, and net-architecture and execution.

Research Projects Software
Prism (ISPASS'18)

- FOSS framework to abstract application workloads for multi-platform, event-driven, generalized workload analysis
- Enable workload-guided projects in thread-mapping, ASIC design, and Network-on-Chip routing
- Leverages Valgrind and DynamoRIO instrumentation, with experimental perf support
- Developer and Maintainer

SynchroTrace (TACO'18)

- Speed up cache-, memory-, and interconnect-oriented gem5 simulation up to 18x for large design space exploration of uncore
- Inter-thread dependencies and Pthread/OpenMP synchronization captured via Prism, replayed in gem5
- Developer and Maintainer

Publications

- Karthik Sangaiah, Michael Lui, Ragh Kuttappa, Mark Hempstead, and Baris Taskin, "*SnackNoc: Processing in the Communication Layer*", Proceedings of the IEEE International Symposium on High-Performance Computer Architecture (HPCA), February 2020.
- M. Lui, K. Sangaiah, M. Hempstead, and B. Taskin, "*Towards Cross-Framework Workload Analysis via Flexible Event-Driven Interfaces*", Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), April 2018.
- K. Sangaiah, M. Lui, R. Jagtap, S. Diestelhorst, S. Nilakantan, A. More, B. Taskin, and M. Hempstead, SynchroTrace: "*Synchronization-aware Architecture-agnostic Traces for Light-Weight Multicore Simulation of CMP and HPC Workloads*", ACM Transactions on Architecture and Code Optimization (TACO), April 2018.
- V. Pano, S. Lerner, I. Yilmaz, M. Lui, and B. Taskin, "*Workload-Aware Routing (WAR) for Network-on-Chip Lifetime Improvement*", Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), May 2018.

Presentations

- M. Lui, M. Hempstead, and B. Taskin, *Simplifying Workload Analysis*, Poster presented at ARM Research Summit, September 2017.
- M. Lui, K. Sangaiah, M. Hempstead and B. Taskin, *Sigil2 and SynchroTrace: Flexible Workload Profiling and Fast Memory-NoC Simulation*, Tutorial presented at IEEE International Symposium on Workload Characterization (IISWC), September 2016.
- M. Lui, V. Pano, M. Hempstead and B. Taskin, *Sigil and SynchroTrace: Communication-Aware Workload Profiling and Memory–NoC Simulation*, Tutorial presented at IEEE International Conference on Computer Design (ICCD), October 2015.
- S. Nilakantan, M. Lui, and M. Hempstead, *Sigil and SynchroTrace: Communication-Aware Workload Profiling and Memory–NoC Simulation*, Tutorial presented at IEEE International Symposium on Workload Characterization (IISWC), October 2015.
- S. Nilakantan, M. Lui, P. Mokri, and M. Hempstead, *Sigil: A Tool for Assisting Accelerator Selection*, Tutorial presented at IEEE International Symposium on High-Performance Computer Architecture (HPCA), February 2015.

Teaching and Mentoring Experience

Adjunct Instructor, Summer 2016, Summer 2017
Department of Computer and Electrical Engineering, Drexel University

- ECEC-353: Systems Programming

Teaching Assistant, Fall 2014-Present
College of Engineering, Drexel University

- ENGR-201: Evaluation and Presentation of Experimental Data I
- ENGR-202: Evaluation and Presentation of Experimental Data II
- ENGR-231: Linear Engineering Systems
- ENGR-232: Dynamic Engineering Systems
- ECE-105: Programming for Engineers II
- ECE-200: Digital Logic Design
- ECEC-201: Intro to C Programming
- ECEC-302: Digital Systems Projects
- ECEC-355: Computer Architecture
- ECEC-356: Embedded Systems
- ECEC-357: Intro to Computer Networks
- ECEL-304: ECE Lab 4

Senior Design Mentor, Academic Year 2016-2017
College of Engineering, Drexel University

- ArchEval: an Application for Architectural Evaluation using Gem5 and SynchroTrace

Undergraduate Research Mentor, Spring 2017-Present
Drexel University

- Project based on LLVM-based instrumentation of multi-threaded applications

Volunteer Instructor, Winter 2017-Present
Coded by: Kids, Philadelphia, PA

- Introduce children and adolescents to programming concepts in weekly sessions
- Use Codio cloud IDE for C, C++, Java, Javascript, HTML, and CSS based projects

Industry Experience

Intel, Graphics Hardware Engineer, August 2012-April 2014

- Investigate corner cases and oversights in media encode (H.264/MP2/VP8) architecture and interaction with external features including power management and cache
- Generate graphics microcode level tests to validate functionality of media encode accelerator architecture
- Detected and debugged functional and hang failures on architecture simulation source, FPGA cluster emulation, and silicon via custom tool flows specific to the platform that allowed access to internal memory views and system snapshots
- Led review meetings with architectural, design, and driver engineers to ensure sufficient coverage of media encode fixed function hardware
- Maintained communication with project stakeholders to assure validation schedule would execute in time for RTL freeze to be fabricated without logic bugs

- Created and maintained various tools for media validation team, including execution automation programs and scripts, and graphics microcode coverage analyzer
- Managed intern by leveraging existing workloads and collaborating on team improvements such as test database backend/frontend improvements
- Set up and maintained DokuWiki web server for team to accelerate and ease knowledge-sharing to reduce duplicated effort

Interdigital, Engineering Co-op, Hardware, LTE, March 2011-September 2011

- Created software and hardware test-benches for FPGA implemented LTE IP components
- Designed and tested new FIR filter memory components for LTE IP meeting 3GPP Rev. 8 specifications
- Synthesized and analyzed Verilog and VHDL test-benches for component verification
- Aided software team in software/hardware integration of PUSCH/PUCCH functionality on ARM/FPGA testbed

Drexel University, Student Worker Sys Admin, CS Dept, September 2010-March 2011, September 2011-Present

- Maintained research and departmental servers via various monitoring and logging tools
- Debugged various IT evils on faculty and staff computers, including file sharing and e-mail solutions
- Generated metric analysis framework utilizing Nagios monitoring and RRDtool logging

Industry Experience (cont'd)

Lockheed Martin MS2, BMD 5.0 C&D, September 2009-March 2010

- Assessed SysML model for accuracy and maintained with the most recent specifications
- Collaborated in a team environment to aid in Matlab simulation of BMD and AAW track filter processing
- Refactored C++ code for Matlab environment with Matlab mex files, for efficient study of simulation algorithms
- Independently performed study of the integrity of changes to BMD Impact Point/Area of Uncertainty calculations

Lockheed Martin MS2, BMD 5.0 C&D, September 2008-March 2009

- Fully developed a Matlab model to test and add additional functionality to AOU (Area of Uncertainty) specifications
- Supported testing of software in new hardware configurations to be placed on current/upcoming Navy Destroyers/Cruisers
- Reviewed proprietary specification and requirement documents for readiness of Navy delivery
- Supported in troubleshooting modernization implementation of updated COTS hardware for Naval vessels

Miscellaneous Projects Experience

Nuclear Reactor Simulator utilizing Microsoft Kinect

- Featured in "Video Games in the Classroom", Nuclear News, January 2013, an American Nuclear Society Publication
- Collaborated with nuclear reactor training site for authentic design input and engineering concerns
- Coordinated with a multidiscipline team integrating reactor modeling, image processing, and GUI, in weekly team meetings
- Designed GUI components, functionalities, and textures, for ergonomic use, utilizing OpenGL in C++
- Worked toward implementing a robust image processing algorithm for detection of hand grabbing gestures

Professional Memberships

- IEEE Society Membership

Awards and Funding

- Samsung Global Research Outreach — Fall 2014 – Fall 2015
- Drexel University Dean's Scholarship — September 2007 – June 2012
- Drexel University College of Engineering Teaching Fellowship — September 2014 – June 2015
- The Koerner Family Fellowship — 2018

References

- **Dr. Baris Taskin**
  Professor, Department of Electrical and Computer Engineering
  Drexel University, Philadelphia, PA
- **Dr. Mark Hempstead**
  Associate Professor, Department of Electrical and Computer Engineering
  Tufts University, Medford, MA
- **Suganya Parthasarathy**
  Program Manager, Visual and Parallel Computing Group
  Intel, Folsom, CA