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TSV-Based Antenna for On-Chip Wireless Communication

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Abstract: On-chip wireless interconnects provide signal broadcasting and link shortcuts for improved latency and throughput, useful considering the increase of the number of processing elements on a chip. In this work, a through-silicon via antenna (`TSV_A`) for on-chip wireless communication is proposed. `TSV_A` significantly improves the wireless interconnect performance over current solutions of on-chip antennas, which occupy a large area of the chip and are not capable of far-reaching transmission. Printed circuit board prototypes (PCB) are designed and fabricated to validate the proposed `TSV_A`. The PCB prototype of the `TSV_A` has an insertion loss of 5 dB to 10 dB at a distance of ≈20mm, measured in PCB and validated with high fidelity 3D finite element method simulation results. `TSV_A` has improved path loss, smaller size, and lower manufacturing costs due to well-established TSV fabrication process for 3D-ICs. Projections for an on-chip 3D IC operation indicate up to 40 dB improved signal strength compared to other on-chip antennas, with an insertion loss of ≈3-5 dB up to a 30mm distance.

1 Introduction

Network-on-Chip (NoC) are be the most viable alternative to an interconnect bus for the scalability of on-chip computing systems [1–3]. Wireless Networks-on-Chip (WNoCs), through the inclusion of on-chip antennas, are introduced to improve the performance of long-distance communication within a chip [4–6]. The inclusion of on-chip antennas (first studied in [7]) creates shortcut links capable of traversing the entire NoC without congesting the wire-based interconnect. Additionally, wireless NoCs are exceptional for multicast and broadcast support for applications dominated by multicast traffic. Larger scale architectures like multi-die systems or multichip modules that are emerging [8, 9] will benefit from high-speed transmission that on-chip antennas provide. Wireless NoCs allow for improved latency of long-distance data transmission but the main issues are the prohibitive size and the signal attenuation (i.e. path loss) of current antennas in literature used for WNoCs.

Lin et al. [10] demonstrate fabricated (90nm–130nm technology) dipole [11] and zig-zag [12] antennas to be used in the WNoC. Timoneda et al. [13] perform 3D FEM simulations to study millimeter-wave propagation within a computer chip package. The performance of a monopole antenna for a WNoC application are evaluated in [14, 15]. Yu et al. [16] propose (and fabricated in 65nm bulk CMOS process) an on-off keying (OOK) transceiver which consume only 1.2 pJ/bit at a data rate of 16 Gb/s operating at 60 GHz. More et al. [17] investigate signal integrity and interference: demonstrating that transmission gain between on-chip antennas is mostly unaffected by the presence of local metal interconnects and the signal integrity on the metal interconnects are not adversely impacted by the on-chip antennas.

The most prominent on-chip antenna designs for on-chip wireless communication are the planar log-periodic [18, 19] and meander [20, 21] which have a surface-propagation of the EM waves of the antenna. The main detriment of these antennas, and surface-propagation in general, is the poor signal attenuation (i.e. path loss) even at small distances of 5mm. With the increase of die size, and particularly the introduction of non-monolithic multi-die chips, there is a pressing need for improved EM radiation efficiency and transmission gain at further distances, for instance, up to 30mm. A novel on-chip wireless communication interconnect using through-silicon-vias (TSVs) as antennas is presented in this work. The proposed TSV-Antenna labeled `TSV_A` propagates the signal through the silicon substrate of the die, rather than the surface, creating a guidance medium that is capable of transmitting at further distances than the normal surface-propagating antennas. The improved signal performance leads to low power dissipation and added wireless transmission distance, ideal for future large-scale processors.

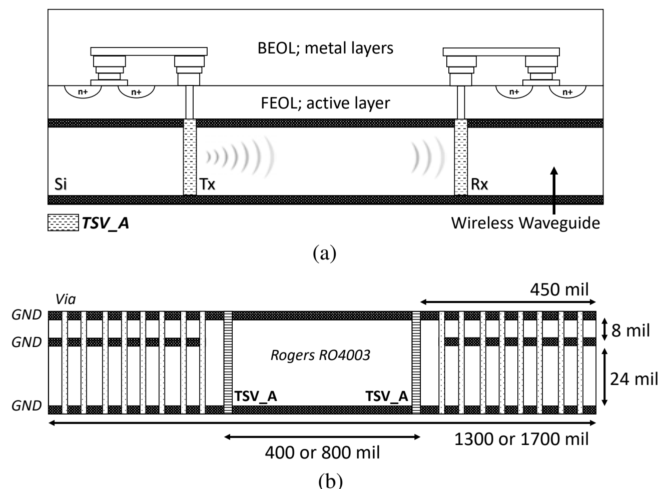

Fig. 1: (a) Illustration of a 3D IC die cross-section with 2 TSV_As labeled Tx and Rx. (b) Cross-section of the PCB prototype with 2 PCB TSV_A.

An illustrative (not to scale) representation of two `TSV_As` communicating is shown in Figure 1(a). The two TSVs are shown as the transmitter (Tx) and the receiver (Rx) unit. The silicon substrate layer with optional top and bottom ground planes acts as a wireless waveguide for the signal generated from the `TSV_A`. Fabrication of the `TSV_A` follows the standard 3D-IC procedures for typical TSVs. The front-end-of-line (FEOL) and back-end-of-line (BEOL) layers are compliant with common manufacturing processes as well as modern application-specific integrated circuit (ASIC) flow, with no influence on those processes. The optional top and ground planes are introduced for even further improved signal integrity, and manufactured using common post-IC-manufacturing processes. Antennas with glass substrate propagation for 3D ICs are proposed in [22, 23].

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HFSS simulations show a carrier frequency between 70 and 90 GHz, with a bandwidth of ≈10 GHz.

The experimental validation of TSV_As are performed with 1) 3D FEM simulations of PCB and 3D-ICs TSVs, and 2) Measurements of representative (larger feature size) PCB implementations, as opposed to costly 3D IC manufacturing. To that end, PCB TSV_As, as shown in Figure 1(b) are manufactured and measured. The PCB implementation is sized to reflect the ratios and distances expected in a 3D IC implementation, with state-of-the-art TSV dimensions projected onto a PCB size. For instance, the material for the PCB substrate, Rogers RO4003, is selected to have similar tangent loss as the 3D IC substrate. The height of the PCB is selected to reflect the aspect ratio of TSVs as well.

The design of TSV_As is detailed in Section 2. The details of the TSV_A PCB prototypes with design choices to make it "representative" to the IC implementation, as well as the propagation studies are presented in Section 2. The PCB measurement results and interpretation of results are presented in Section 4. Finally, summary and conclusions of the work are presented in Section 5.

2 Proposed IC TSV Antenna (IC TSV_A)

The design of the proposed TSV_A is based on a typical disc-loaded monopole antenna. A TSV acts as the main radiating part of the monopole antenna. The detailed model of the TSV_A is shown in Figure 2.

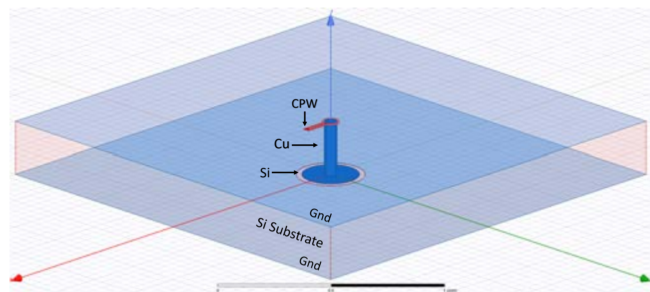

Fig. 2: HFSS design of the TSV_A in 3D IC.

The TSV_A is placed inside the layer of silicon (Si) substrate. Top and bottom ground planes are added to increase transmission gain. In HFSS simulations, the TSV material is selected to be copper (Cu), however any conductive material in varying TSV implementations could theoretically be used as the main radiating part of the monopole antenna. The top ground plane acts as a reflective surface for the wave generated by the TSV_A and prevents interference between the TSV_A wave and the active Si and metal layers. The undoped silicon layer acts as a waveguide that provides the main path for electromagnetic (EM) waves. In simulations, the relative dielectric constant (ε_r) used for the Si substrate is 11.7. An optional bottom plane serves to improve the channel quality. The cylindrical disc created from the etching at the bottom of the TSV_A is used for impedance matching to improve the overall strength of the signal.

On-chip wireless communication is projected at the mm-wave communication range [24, 25]. A target frequency of 60GHz is selected in this manuscript to conform to this range. It is feasible to choose different resonant frequencies with geometrical changes, if desired, or to adhere to guidelines imposed by manufacturing or to limit interference with other wavelengths in the medium. HFSS simulations at 60 GHz resonant frequency are performed to demonstrate the signal performance of TSV_A in communication quality over increasing distances between pairs of TSV_As. Path loss analysis is performed for the TSV_A and compared against the planar log-periodic [18, 19] and meander [20, 21] antenna. The results of the HFSS path loss evaluation are shown in Figure 3. The two TSV_As (Tx and Rx) are placed at increasing distances (1.25–30 mm) from each other, labeled as Tx-Rx distance on the x axis. The TSV_A has

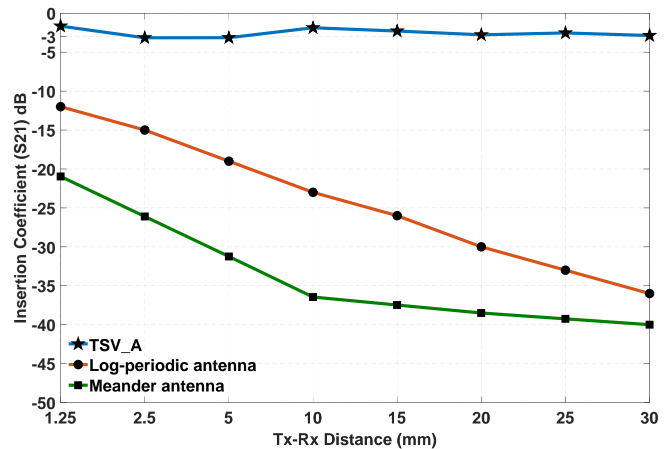

Fig. 3: HFSS simulation of insertion loss (S21) versus distance for IC TSV_A compared to different on-chip antennas.

an almost constant and very low *3 dB* path loss due to the silicon medium, top and bottom ground planes, acting as a wireless waveguide for the signal. The planar log-periodic and meander antennas suffer from exponential increase in path loss (up to 40 dB for the meander and up to 35 dB for the log-periodic antennas) due to the surface-propagation of the EM field.

Table 1 On-chip Antenna Comparison

D	Structure	Frequency	Return Loss	Insertion Loss
10mm	**IC TSV_A**	60 GHz	-30 dB	**-3 dB**
	Zig-zag [26]	60 GHz	-35 dB	-30 dB
	TGV [27]	62 GHz	-37 dB	-20 dB
	Monopole [14]	57 GHz	-40 dB	-25 dB
	Log-Periodic [18]	44, 60 GHz	-15, -15 dB	-23 dB
	Meander [20]	18, 24 GHz	-19, -13 dB	-36 dB
20mm	**IC TSV_A**	60 GHz	-30 dB	**-3 dB**
	Zig-zag [26]	60 GHz	-35 dB	-40 dB
	TGV [27]	62 GHz	-34 dB	-25 dB
	Monopole [14]	57 GHz	-40 dB	-30 dB
	Log-Periodic [18]	44, 60 GHz	-15, -15 dB	-30 dB
	Meander [20]	18, 24 GHz	-19, -13 dB	-40 dB

A comparison of on-chip antennas, including the proposed TSV_A, is shown in Table 1. Two sets of data are shown: One for the Tx-Rx distance of 10mm and another for 20mm. The resonant frequencies, return loss, and insertion loss of the TSV_A are compared against all current WNoC antenna solutions in literature: i) the zig-zag antenna [26], ii) the glass interposer antenna (TGV) [22, 23, 27], iii) the monopole antenna [14], iv) the planar log-periodic [18] antenna, and v) meander [21] antenna. It is shown that TSV_A at both distances has an insertion loss of -3 dB, which is orders of magnitude smaller than all other on-chip antennas surveyed. Specifically, the insertion loss of the TSV_A (3db) is up to 17 dB better than the best solution in literature, 20 dB for the TGV [27] at 10mm distance. At a 20mm distance, the insertion loss is up to 22 dB better than that of the TGV. Improved insertion loss provides several benefits, including: i) low power consumption, ii) the removal of low-noise amplifiers (LNAs), and, iii) TSV_A position flexibility during design-time. These three factors are the key to improving the performance of future large-scale multi-chip architectures for next-generation workloads.

3 PCB Prototype of TSV_A Design (PCB TSV_A)

PCB prototypes of the TSV_As are manufactured, preferred over a 3D IC due to the prohibitive cost and long turnaround time of manufacturing a prototype in a 3D IC environment. The PCB measurement results are used to characterize the TSV_As, and to

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prove the fidelity of HFSS results for TSV_A implementations in IC integration.

The PCB prototypes use the Rogers RO4003C material with a dielectric constant ε_r of 3.55 and a dielectric tangent loss of 2.7×10^{-3}, high resistivity (HR) silicon for 3D ICs has up to $10\ \mathrm{k\Omega \cdot cm}$ which corresponds to a conductivity of $1 \times 10^{-2}\ \mathrm{S\,m^{-1}}$. Tangent loss of HR silicon is calculated as [1]:

$$tan\ \delta = \frac{\sigma}{\omega * \varepsilon}, \tag{1}$$

where σ is the electrical conductivity of the medium, ω is the angular frequency, and ε represents permittivity of the medium.

If a resistivity of $3\ \mathrm{k\Omega \cdot cm}$ is assumed for silicon (ε_r of 11.7) in 3D ICs then the tangent loss at 20 GHz is calculated as 2.6×10^{-3}, approximately the same as the Rogers RO4003C material. This similarity of tangent loss value is the rationale behind evaluating the TSV_A PCB prototype as a surrogate for the (prohibitively costly) 3D IC TSV_As.

A cross-section of the PCB layers in the manufactured prototype is shown in Figure 1(b). In order to accurately capture the performance of an IC TSV_A model depicted in Figure 2, the PCB implementation of the TSV_As has been resized as shown in Figure 5, primarily to match the change in ε_r from silicon to RO4003C. In addition to top and bottom ground planes (1mil each), an intermediate ground plane is part of the structure in order to optimize the CPW and minimize the number of excited modes. Additional via across the CPW are added to improve signal transfer to the TSV_A.

The PCB TSV_A manufacturing and measurement are utilized to also assess the impact on channel quality of i) TSV_A geometries, ii) transmission distance and iii) the physical channel. To those ends, the PCB prototype includes three different TSV_A structures measured at two arbitrary distances, 400mil (≈10mm) and 800mil (≈20mm) with respective board lengths of 1300mil and 1700mil. Also included for thoroughness, is a CPW feed line that goes over the entire distance of the boards, in order to differentiate the insertion loss incurred from a typical CPW as opposed to the proposed TSV_A. The CPW structure is detailed in Section 3.1. The three TSV_A structures are detailed in Section 3.2.

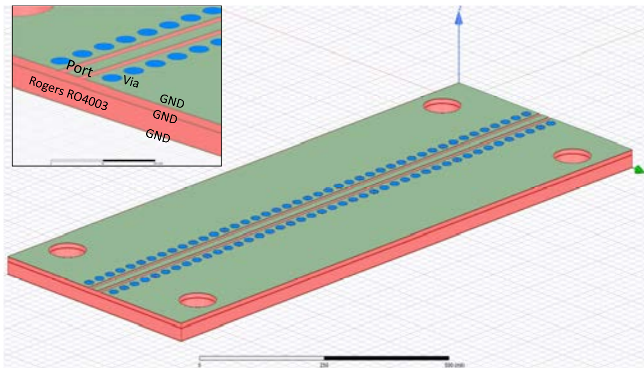

Fig. 4: CPW used to feed the signal to the PCB TSV_A.

3.1 Co-Planar Waveguide Design

A CPW is build in order to provide the signal to the TSV_As. End launch connectors (50 GHz) from Southwest Microwave [28] are used to connect the PCB prototype to the VNA (PNA-X N5247A). A CPW length of 450mil is selected for each port to adequately distance the end launch connectors from the TSV_As. The full-distance CPW is shown in Figure 4, which includes a magnified look at the connection to the end launch connectors. The trace width of the CPW is 17mil, substrate thickness is 8mil (intermediate ground plane of the PCB acts as the bottom of the CPW) and the spacing between the top ground plane and the trace width is 10mil on both sides.

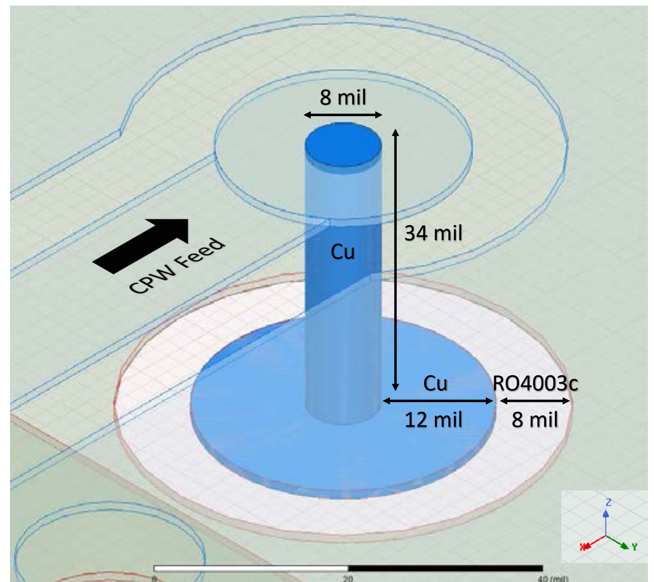

Fig. 5: PCB TSV_A structure and size.

3.2 PCB TSV Antenna Design

The structure for the TSV_A PCB prototype is presented in Figure 5. Both the IC and PCB TSV_A have the same design, although the PCB prototype of the TSV_A is scaled up to operate at lower frequencies due to the different material and PCB sizing limitations [29]. The height of TSV_A is 34mil and the perimeter is 8mil. The gap size is 8 mil and the disc size is 12mil. The PCB prototypes include three different TSV_A structures:

- The first PCB structure, shown in Figure 6(a), has two TSV_As connected through the CPW feed line. Two arbitrarily selected distances are manufactured: 400mil and 800mil.
- The second PCB structure, shown in Figure 6(b), has additional vias placed at a 90° angle with respect to the TSV_A. This structure is included in order to provide a divide between the CPW feed and the actual TSV_A in case of possible interference by the VNA or additional excited modes.
- The third PCB structure with TSV_As, shown in Figure 6(c), has additional vias placed at a 45° angle with respect to the TSV_A. These via provide additional directivity for the radiation emitted by the TSV_A.

The overall fabricated PCB prototype board housing the TSV_A structures is shown in Figure 7. The PCB structures are connected to the VNA via end-launch connectors as shown in Figure 8. Both transmission distances and all four structures (including the CPW feed line in Figure 4) are fabricated on the same board. Additional via are added to the sides of each structure to keep the structures isolated from each other.

4 Simulated and Measured Results of PCB TSV_A

A two step verification process is adopted:

- Verify, through PCB fabrication, that the TSV_A structure is capable of wireless transmission with minimal insertion loss.
- Verify, through simulated vs measured results comparison, that the fidelity of HFSS finite element method simulation permits further design exploration with TSV_As without PCB or 3D IC fabrication.

Measured results of the PCB structures are shown in Table 2. Measured data include approximate resonant frequencies, return loss and insertion loss. The measurements are presented for both

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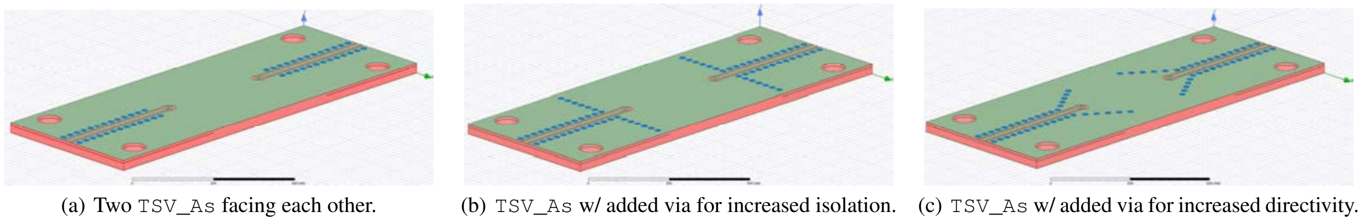

(a) Two TSV_As facing each other. (b) TSV_As w/ added via for increased isolation. (c) TSV_As w/ added via for increased directivity.

Fig. 6: HFSS models of PCB TSV_A structures fabricated.

Fig. 7: Photo of all fabricated PCB structures next to a US quarter. Each square in the background has 5mm sides.

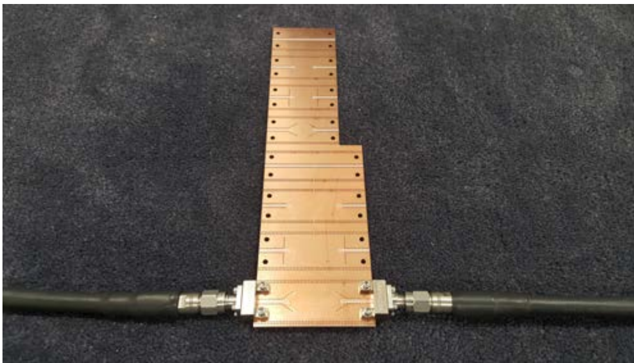

Fig. 8: Photo of one of the PCB structures connected to the VNA (PNA-X N5247A) via the SMA end-launch connectors for measurement purposes.

Table 2 PCB Prototype Measured Results

D	PCB Structure	Frequency	Return Loss	Insertion Loss
10mm	CPW	20–50 GHz	30–50 dB	2–5 dB
	TSV_A	21, 33, 41 GHz	10, 15, 15 dB	7, 6, 15 dB
	TSV_A w/ 90° via	21, 33, 37 GHz	14, 12, 16 dB	5, 10, 8.5 dB
	TSV_A w/ 45° via	24, 30, 35 GHz	10, 15, 12 dB	6, 9, 6 dB
20mm	CPW	20–50 GHz	35–55 dB	2–5 dB
	TSV_A	21, 33 GHz	14, 20 dB	4.5, 16 dB
	TSV_A w/ 90° via	21, 29, 37 GHz	20, 19, 18 dB	4, 8.5, 12 dB
	TSV_A w/ 45° via	29, 34, 37 GHz	10, 18, 20 dB	8, 12, 8.5 dB

10mm (400mil) and 20mm (800mil) transmission distances and for the four following PCB protoypes: 1) The CPW structure at two different sizes, 2) the TSV_A structure without additional vias, 3) the TSV_A structure with additional vias at a 90° angle, 4) the TSV_A structure with additional vias at a 45° angle. It is shown that PCB TSV_A at 20mm distance performs up to 30 dB better than the planar log-periodic [18] and meander [20] antennas, respectively. The results in Table 2 for these four PCB prototypes are elaborated in the following four respective sections.

4.1 CPW Results

The CPW structure is shown in Figure 4. A comparison of the simulated and measured results of the CPW for both dimensions is shown in Figure 9. Insertion loss of the CPW is between 2 dB and 5 dB, depending on the operating frequency, for both dimensions. Although the measured results are similar to the simulated results, there is a larger insertion loss in measurements at higher frequencies (above 35 GHz) for both dimensions. In lower frequencies (below 35 GHz), the change in insertion loss is minimal (≈1 dB). Return loss (S11) is also impacted at higher frequencies, deviating by ≈10 dB from the simulated results.

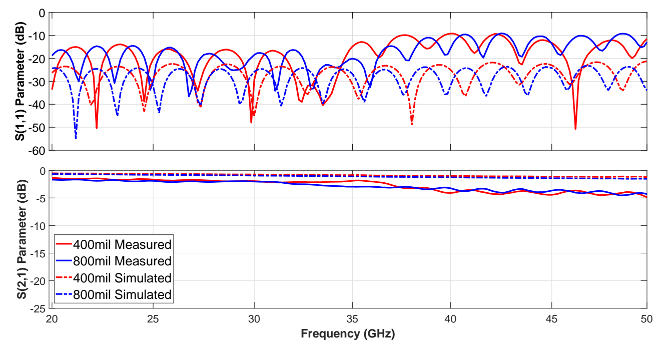

Fig. 9: Simulated and measured results of the CPW on PCB.

4.2 PCB TSV_A Results

Measured and simulated results of the first TSV_A structure for both dimensions are shown in Figure 10. The major *measured* resonant frequency for the 400mil distance is ≈33 GHz, as shown in Figure 10(a). The return loss for this frequency is ≈15 dB and the insertion loss is ≈6 dB. Note that the insertion loss includes the loss from the CPW feed, therefore actual loss from the TSV_A alone is even lower. The simulated results have a minor shift in frequency for both return and insertion loss, visible around 40 GHz (S11) and 25 GHz (S21).

The major *measured* resonant frequencies for the 800mil distance are ≈21 GHz and ≈33 GHz, as shown in Figure 10(b). These resonant frequencies match the previous structure, although insertion loss drops to ≈16 dB for the 33 GHz resonant frequency. The minimum insertion loss is ≈4.5 dB around 21 GHz, which matches the first resonant frequency. Simulated evaluations manage to closely match the S21 peaks in the 20 GHz to 25 GHz, although a small shift in frequency is present. Magnitude-wise, FEM simulations appear to be accurate on and around the resonant frequencies (for both 400mil and 800mil structures) and ≈10dB more optimistic in other regions. The discrepancy in measured and simulated results is attributed to the simulation resolution and the modeling of multipath interference (both destructive and constructive).

4.3 PCB TSV_A with 90° Angle Vias Results

Measured and simulated results of the second TSV_A structure for both dimensions are shown in Figure 11. These structures have additional via lined up at a 90° angle with respect to the main TSV_A, as shown in Figure 6(b). The major *measured* resonant frequencies for the 400mil distance are similar to the TSV_A structure in Section 4.2. Insertion loss appears to be consistently less than 10 dB for each of the major resonant frequencies below 40 GHz. The TSV_A dimensions are optimized for these frequency ranges, therefore a small insertion loss is expected at these resonant frequencies. The additional via are added to provide a divide between the

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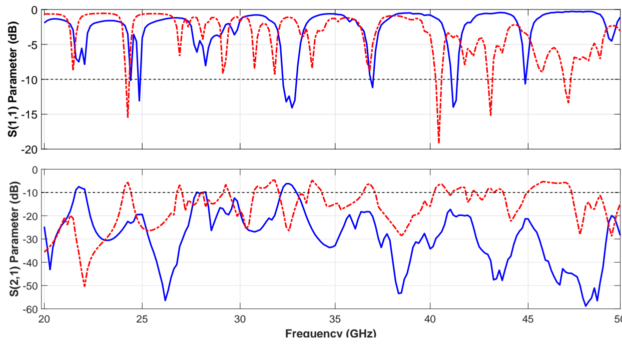
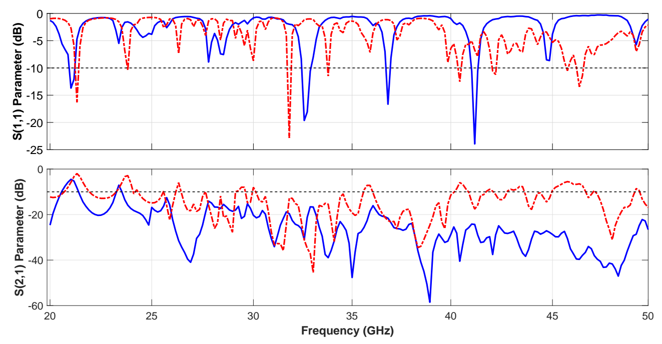
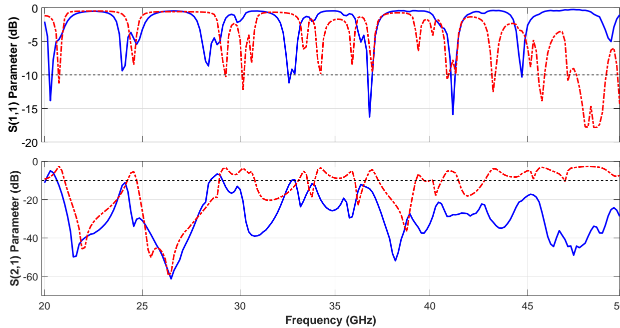


(a) TSV_As at 400mil distance.

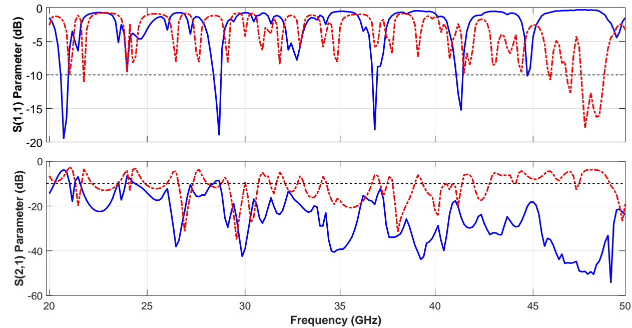


(b) TSV_As at 800mil distance.

Fig. 10: Measured (solid blue) vs simulated (dashed red) results of the TSV_A without additional via.

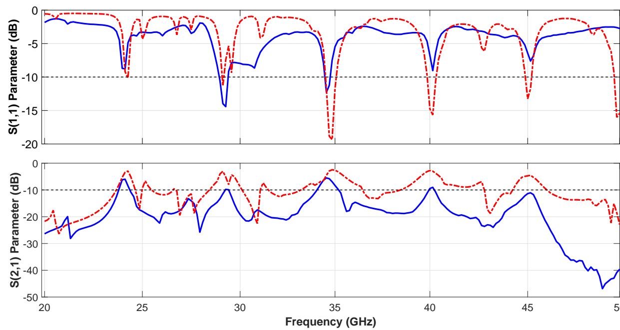


(a) TSV_As at 400mil distance.

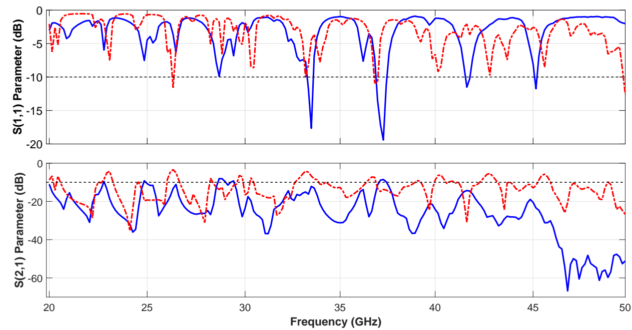


(b) TSV_As at 800mil distance.

Fig. 11: Measured (solid blue) vs simulated (dashed red) results of the TSV_A with additional via at a 90° angle.



(a) TSV_As at 400mil distance.



(b) TSV_As at 800mil distance.

Fig. 12: Measured (solid blue) vs simulated (dashed red) results of the TSV_A with additional via at a 45° angle.

CPW feed and the actual TSV_A to avoid possible interference from the VNA or additional excited modes. Simulation results are more closely matched to the measured results due to the isolation from the CPW, therefore decreasing simulation complexity and improving simulation accuracy.

The major *measured* resonant frequencies for the 800mil distance are ≈21 GHz, ≈28 GHz, and ≈37 GHz, as shown in Figure 11(b). The minimum insertion loss is ≈4 dB around 21 GHz and the maximum insertion loss (out of the resonant frequencies) is ≈12 dB around 37 GHz. At lower frequencies (below 40 GHz), simulation results of insertion loss appears to be match the measured results. In addition to performing discrete measurement of each frequency as opposed to the fast or interpolation methods, the HFSS structure mesh resolution can be increased to improve the accuracy of the FEM simulations.

4.4 PCB TSV_A with 45° Angle Vias Results

Measured and simulated results of the third TSV_A structure for both dimensions are shown in Figure 12. These structures have additional via lined up at a 45° angle with respect to the main TSV_A, as shown in Figure 6(c). The TSV_A is based on a disc-loaded monopole antenna therefore it radiates in all directions. The additional via at a 45° angle improves signal directivity and minimizes coupling. The major *measured* resonant frequencies for the 800mil distance are ≈24 GHz, ≈30 GHz, and ≈35 GHz, as shown in Figure 12(a). The return loss for these frequencies is between 9 dB and 15 dB and the insertion loss is ≈5 dB at 21 GHz. The simulated results match the measured results closely and all resonant frequencies are accounted for in the HFSS results. Magnitude-wise, HFSS is optimistic in the higher frequency ranges (above 35 GHz) but matches magnitude in the lower frequency ranges (below 35 GHz).

The major *measured* resonant frequencies for the 800mil distance are ≈29 GHz, ≈34 GHz, and ≈37 GHz, as shown in Figure 12(b). Insertion loss appears to be consistently less than 12 dB for each

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of the major resonant frequencies. The 45° angled via provide additional directivity to the main TSV_A, thus improving insertion loss at further distances up to ≈8 dB. The additional directivity can be adapted to isolate the signal and provide multi-band operation in a Network-on-Chip. Simulations results appear to be pessimistic when calculating S11 and closely matched when computing S21. Simulated results of higher frequencies are not as accurate and tend to be optimistic in computing insertion loss.

VNA measurements support the conclusion that PCB TSV_A exhibits excellent signal attenuation (an insertion loss as low as 5 dB up to 20mm transmission distance). FEM evaluation of 3D IC TSV_A indicates insertion loss as low as 3 dB up to 30mm transmission distance, consistent with measurement data.

5 Conclusions

This work evaluates a through-silicon via antenna (TSV_A) based on the disc-loaded monopole antenna. TSV_A propagates the signal through the silicon substrate of the die, rather than the surface, creating a guidance medium that is capable of transmitting at further distances than the normal surface-propagating antennas. The improved signal performance leads to low power dissipation and added wireless transmission distance, ideal for next-generation scalable compute packages.

In order to verify functionality and performance, a PCB prototype is fabricated and measured with a VNA. Measurements results indicate that the TSV_A is capable of transmission up to 800mil (20mm) distance with only 5 dB to 10 dB insertion loss. Multiple TSV_A structures with additional via to improve directivity are measured and evaluated, improving insertion loss from the standalone TSV_A. Finite element method simulations, executed through HFSS, appear to match the measured results in lower frequencies. Higher frequencies require further mesh refinement and increased simulation resolution to match measurements. These high fidelity HFSS simulations are used to project the performance of TSV_As in a 3D IC: 30 dB improved insertion loss compared to other on-chip antennas, with an insertion loss of ≈3dB up to 30mm distance.

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